Code No: 137CV

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, March - 2021
FPGA PROGRAMMING
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

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1.a) With neat sketch explain Altera max 5000 series CPLD.
b) What is a structured ASIC? How does this compare and differ from the traditional ASIC and the PLD? [7+8]

2.a) List out the applications of FPGAs.
b) Draw and explain Simple SRAM-Programmable FPGA Architecture. [5+10]

3.a) What is UDM and UDM-PD? Compare them.
b) What are the floating nodes? How to design them? [7+8]

4.a) Discuss the VLSI design issues and design trends.
b) What is the difference between structural and behavioral models in VHDL programming? [7+8]

5.a) Write the Verilog syntax for CASE & LOOP statements.
b) Explain the Structure of the dataflow description with suitable diagram. [7+8]

6.a) Compare the Structural level Descriptions and Switch level Descriptions in Verilog programming.
b) Write a short note on serial and parallel combinations of switches. [8+7]

7.a) Write a VHDL program for half adder.
b) Discuss about declarations of bidirectional switches in VHDL. [8+7]

8.a) Draw and explain the procedures structure and its syntax.
b) Discuss about any two examples of Procedures and Tasks. [7+8]

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