Code No: 115EB

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year I Semester Examinations, February/March - 2016
LINEAR AND DIGITAL IC APPLICATIONS
(Common to ECE, BME)

Time: 3 hours

Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

Part- A

(25 Marks)

1.a) Give the ideal values and practical values of various op-amp parameters. [2]
 b) Define thermal drift and slew rate. [3]
 c) Write the applications of 555 timer in astable mode. [2]
 d) What are the modes of operation of a timer? [3]
 e) Explain the principal of weighted resistor type DAC. [2]
 f) List the specifications of DAC. [3]
 g) Define Priority Encoder. [2]
 h) Write the Classification of Integrated Circuits. [3]
 i) Name different Types of ROMS. [2]
 j) List the applications of ROMs. [3]

Part-B

(50 Marks)

2.a) What are the three differential amplifier configurations? Compare and contrast these configurations.
 b) Explain frequency compensator techniques used in op-amp. [6+4]

OR

3.a) Calculate the effect of variation in power supply voltages on the output offset voltage for an op - amp circuit.
 b) Explain the advantages and disadvantages of ICs. [6+4]

4. Give the functional block diagram of VCO NE566 and explain its working and necessary expression for free running or center frequency. [10]

OR

5.a) Explain the monostable operation of the 555 timer and derive the expression for the period of a pulse generated by the Timer
 b) Design a circuit to generate square waveform using op-amp. [5+5]

6. Draw the block diagram and explain the operation of dual slope A/D converter. What are its advantages and disadvantages? [10]

OR

7.a) Explain the operation of the fastest analog to digital converter. What is the main drawback of this converter? Compare this converter with other types.
 b) Draw the circuit of a Ladder type DAC for 4 bits and derive expression for output voltage. [5+5]

8. Design and explain the following
   a) Basic comparator operation.
   b) Logic diagram for comparison of 2- bit binary numbers. [5+5]

OR

9.a) Design a 2-input NOR gate using CMOS transistors. Explain the operation of the circuit with the help of function table.
  b) Discuss about LED and LCD decoders with drivers. [7+3]

10.a) Draw the internal structure of synchronous SRAM and explain the operation.
   b) Design and explain 1T DRAM Cell. [5+5]

OR

11.a) Explain the functional behavior of Static RAM cell? Show the internal structure of 8×4 static RAM.
   b) Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms. [5+5]

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