Code No: 138EW

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, December - 2020
SYSTEM DESIGN USING FPGAS
(Electronics and Communication Engineering)

Time: 2 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

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1.a)	Explain about three state buffer with example.	
b)	What is mean by HDL? Compare this with other High-level languages.	[8+7]
2.a)	Write the HDL Synthesis Rules in detail.	
b)	Explain about HDL Simulation Environment with suitable examples.	[7+8]
3.a)	Write a VHDL Program for a Half Adder.	
b)	What is the Code Converter? Explain about its working principle.	[8+7]
4.a)	Write a VHDL Program for carry look ahead adder.	
b)	Write a VHDL program for any one Encoder.	[8+7]
5.a)	Write a VHDL code for D latch.	
b)	Write a VHDL code for a 4 - bit Down Counter.	[6+9]
6.a)	Explain about Interrupt Registers.	
b)	Write a VHDL code for SR flip flop.	[7+8]
7.a)	Write a short note on clock divider and gated clock.	
b)	Explain the race around condition with suitable example.	[8+7]
8.a)	Explain about Best-case Timing Analysis.	
b)	Discuss about Post layout Verification.	[8+7]

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