Code No: 137JD

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, October/November - 2020
VLSI DESIGN
(Common to ECE, EIE)

Time: 2 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

1.a) Explain about PMOS transistors steps involved in n-well fabrication process?
b) Compare and contract enhancement and depletion mode of MOS devices. [8+7]

2.a) Demonstrate the mathematical equations that can be used to model the drain current and diffusion capacitances of MOS transistor.
b) Explain in detail about the body effect and its effect in MOS device. [8+7]

3.a) Write the layout design rules and Draw the layout diagram for NAND and NOR gate
b) Discuss in detail with a neat layout, the design rules for a CMOS inverter. [8+7]

4.a) Explain the fundamental units of CMOS inverter.
b) Explain the principle of constant field and lateral scaling. And write the effects of the above scaling methods on the device characteristics. [7+8]

5.a) Define parasitic delay and compare the parasitic delay of common gates for various inputs
b) Describe the fan in and fan out characteristics of CMOS. [8+7]

6.a) Illustrate in detail about Cascade voltage switch logic.
b) Analysis the pseudo nMOS logic gates in detailed. [7+8]

7.a) Illustrate the concepts of faster decoder and sum-addressed decoder circuit.
b) Elaborate the concept of large SRAMs. [8+7]

8.a) With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device.
b) Demonstrate the basic types of programmable elements of PLDs. [8+7]

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