R18

Code No: 156DF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, August/September - 2021

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

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1. List the advantages and disadvantages of CMOS technology over bipolar technology. [15]

2.a) Discuss various forms of pull-up with neat diagrams.
b) Write the basic electrical properties of Bi CMOS. [10+5]

3.a) Explain the steps involved in VLSI design flow.
b) Design the AND and OR gates by using stick diagrams. [10+5]

4.a) Develop stick diagram for 2-input CMOS AND gate.
b) Write a short note on scaling of MOS circuit. [7+8]

5.a) Discuss about the methods for driving large capacitive loads.
b) What is Gate-level design, explain in detail. [7+8]

6.a) Discuss about the choice of fan – in and fan – out selection in gate level design.
b) Write a short note on wiring capacitance. [7+8]

7.a) Explain Barrel shifter with a neat diagram.
b) Design and implement 4-bit ripple carry adder. [7+8]

8.a) Explain CMOS test principles in detail.
b) Compare simple PLDs, CPLDs and FPGAs. [7+8]

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