R18

Code No: 158CT

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, July/August - 2022
SYSTEM ON CHIP ARCHITECTURE
(Electronics and Communication Engineering)

Time: 3 Hours **Max.Marks:75**

Answer any five questions
All questions carry equal marks
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1.a) What is processor architecture? What are the different processor architectures available for processor design?
b) Explain in detail about approach for SOC Design. [8+7]

2.a) Discuss about the procedure for Processor Selection for SOC.
b) Explain in detail about the basic concepts in Processor Micro Architecture. [8+7]

3.a) Write short notes on VLIW and Superscalar Processors.
b) What are vector functional units? List their applications. [8+7]

4.a) Describe overview of SOC external memory.
b) Explain in detail about the Cache Organization. [8+7]

5.a) Write short notes on Split – I and D – Caches.
b) List and explain models of Simple Processor. [8+7]

6.a) Distinguish about Inter Connect Architectures in detail.
b) List and explain Analytic Bus Models. [8+7]

7.a) Explain in detail about the trade-off analysis on reconfigurable Parallelism.
b) Discuss in detail about the Vector Processors. [8+7]

8.a) Describe the Architecture of customizing instruction processor.
b) Mention about the Customizable Soft Processor in detail. [8+7]

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