Code No: 156DF

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, August - 2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max.Marks:75**

Answer any five questions
All questions carry equal marks

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1.a) Explain n-well CMOS Process with necessary sketches.
b) Explain MOS system under external bias with necessary diagram. [8+7]

2.a) Derive the Drain to source current I_{ds} versus voltage V_{ds} relationship for a NMOS Transistor when the transistor is in i) Non-saturated region. ii) Saturated region.
b) Discuss about the MOS transistor figure of merit W_0. [8+7]

3.a) Draw the stick diagram, and layout diagram of NMOS inverter.
b) Draw and explain the CMOS lambda based design rules for transistors and wires. [7+8]

4.a) Draw the stick diagram and mask layout for CMOS two input NOR gate.
b) Discuss CMOS design style. Compare with nMOS design style. [8+7]

5.a) Draw and explain fan-in and fan-out characteristics of different CMOS design technologies.
b) What are the alternate gate circuits are available? Explain any one of item with suitable sketch. [8+7]

6.a) Explain the concept of driving large capacitive loads with, relevant examples.
b) Discuss the inverter delay and propagation delay. [8+7]

7.a) Explain step-by-step subsystem design approach. Consider an example.
b) Compare SRAM and DRAM. [8+7]

8.a) Discuss the overflow of system on chip designs.
b) Explain the FPGA design flow. [7+8]

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